AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double brackets indicating deletions.

LISTING OF THE CLAIMS

1. (CURRENTLY AMENDED) A stacked semiconductor package comprising:

a first semiconductor chip;

a second semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed and at least one bottom corner of the second semiconductor chip is exposed;

at least one first conductor electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and

at least one second conductor electrically connecting the second semiconductor chip to ~~the~~ a frame.

2. (ORIGINAL) The package of claim 1, wherein

the first conductor electrically connects at least one bond pad on the first semiconductor chip with at least one bond pad on the second semiconductor chip.

3. (ORIGINAL) The package of claim 2, further comprising:

a redistribution pattern electrically connecting the bond pad on the second semiconductor chip to a differently positioned bond pad on the second semiconductor chip.

4. (CURRENTLY AMENDED) The package of claim 3, further comprising:

~~a frame supporting~~ a chip package structure supported by the frame, the chip package structure including at least the first and second semiconductor chips; and

at least one second conductor electrically connecting the differently positioned bond pad to the frame.

5. (PREVIOUSLY PRESENTED) The package of claim 4, wherein the second conductor electrically connects the differently positioned bond pad to a bond pad on the frame.

6. (ORIGINAL) The package of claim 1, wherein a plurality of first conductors electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. (ORIGINAL) The package of claim 6, further comprising:

the plurality of first conductors respectively electrically connecting a plurality of bond pads on the first semiconductor chip to a first plurality of bond pads on the second semiconductor chip.

8. (ORIGINAL) The package of claim 7, wherein the plurality of bonds pads on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second semiconductor chip corresponding to the edge of the first semiconductor chip.

9. (ORIGINAL) The package of claim 8, further comprising:

a redistribution pattern electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip, the second plurality of bond pads arranged adjacent to a different edge of the second semiconductor chip.

10. (CURRENTLY AMENDED) The package of claim 7, further comprising:

a redistribution pattern electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip.~~;~~

11. (CURRENTLY AMENDED) The package of claim 10, further comprising:

~~a~~ the frame supporting a chip package structure, the chip package structure including at least the first and second semiconductor chips; and

a plurality of second conductors electrically connecting the second plurality of bond pads on the second semiconductor chip to the frame.

12. (ORIGINAL) The package of claim 11, wherein the frame is one of a printed circuit board and a flexible substrate.

13. (ORIGINAL) The package of claim 11, wherein the frame includes a die pad portion supporting the chip package structure and an inner lead portion to which the plurality of second conductors are electrically connected.

14. (ORIGINAL) The package of claim 13, further comprising:

a sealing resin sealing the first and second semiconductor chips, the redistribution pattern, the first and second plurality of conductors, and a portion of the frame.

15. (ORIGINAL) The package of claim 11, wherein the plurality of first and second conductors are bonding wires.

16. (CURRENTLY AMENDED) A stacked semiconductor package comprising:

a first semiconductor chip;

a plurality ~~number, n,~~ of intermediate semiconductor chips n, where $n \geq 0$,~~; wherein n is an integer greater than or equal to 0;~~ each intermediate semiconductor chip ~~being~~ stacked offset over ~~a~~ the first semiconductor chip ~~located underneath the intermediate semiconductor chip~~ such that a portion of the first semiconductor chip and at least one bottom corner of each intermediate chip ~~underneath~~ is exposed;

a second semiconductor chip, wherein when the expression $n > 0$ is satisfied, the second semiconductor chip is stacked offset over the intermediate semiconductor chips- such that a portion of each intermediate semiconductor chip and at least one bottom corner of the second semiconductor chip are exposed, ~~or~~ and when the expression $n = 0$ is satisfied, the second semiconductor chip is stacked offset over the first semiconductor chip- such that the portion of the first semiconductor chip and the at least one bottom corner of the second semiconductor chip are exposed; ~~such a portion of the topmost intermediate semiconductor chip is exposed;~~

at least one first conductor electrically connecting the exposed portions of the first and intermediate semiconductor chips to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and

at least one second conductor electrically connecting the second semiconductor chip to ~~the~~ a frame.

17. (PREVIOUSLY PRESENTED) The package of claim 16, wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first and intermediate semiconductor chips to a first plurality of bonding pads on the second semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

18. (ORIGINAL) The package of claim 17, further comprising:

a redistribution pattern electrically connecting the first plurality of bond pads on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip.

19. (ORIGINAL) The package of claim 1, wherein the first and second semiconductor chips are a same type of chip.

20. (CURRENTLY AMENDED) A stacked semiconductor package comprising:

a stacked chip structure including an upper semiconductor chip and at least one lower semiconductor chip disposed under at least a portion of the upper semiconductor chip such that at least one bottom corner of the upper semiconductor chip is exposed; and

a redistribution pattern redistributing a first plurality of bond pads on the upper semiconductor chip to a differently positioned second plurality of bond pads on the upper semiconductor chip, the first plurality of bond pads being electrically connected with the lower semiconductor chip.

21. (CURRENTLY AMENDED) A method for fabricating a stacked semiconductor package, comprising:

forming a stacked chip package including at least a first semiconductor chip and a second semiconductor chip stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip ~~is~~ and at least one bottom corner of the second semiconductor chip is exposed;

electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor such that the conductor does not extend beyond a periphery of the first semiconductor chip; and

electrically connecting the second semiconductor chip to ~~the~~ a frame.

22. (CURRENTLY AMENDED) A method for fabricating a stacked semiconductor package, comprising:

forming a stacked chip structure including an upper semiconductor chip and at least one lower semiconductor chip disposed under at least a portion of the upper semiconductor chip such that at least one bottom corner of the upper semiconductor chip is exposed; and

electrically connecting the lower semiconductor chip with a first plurality of bond pads on the upper semiconductor chip; and

forming a redistribution pattern redistributing the first plurality of bond pads on the upper semiconductor chip to a differently positioned second plurality of bond pads on the upper semiconductor chip.